Amendments to the Drawings

The attached sheet of drawings includes changes to Figures 1-2. This sheet, which includes Figures 1-2 replaces the original sheet including Figures 1-2. In amended Figures 1-2, the previously omitted legend "Prior Art" has been added.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

I. Objections to the Drawings

In the OA, Examiner objected to omission of a "Prior Art" legend with reference to Figures 1-2. Accordingly, a Prior Art legend has been added to Figures 1-2 as shown the Appendix following page 20 of this Response. Thus, the objections to the Drawings have been obviated.

II. Objections to the Specification

Examiner objected to the Specification in the OA, page 14, line 4. Accordingly, Applicant amended the specifications paragraphs, 004, and 0026 were amended to correct minor informalities. More particularly, paragraphs 004 and 0026 of Applicant's Specification were amended to correct minor informalities relating to "input" terminal 14 of the inverter 12 (¶004) and "drain" region 404 of the third N-type transistor (¶0026), thereby obviating Examiner's rejections.

!!!. Objections to the Claims

Examiner objected to Claims 10 and 14 as containing several informalities. Accordingly, claims 10 and 14 were amended to obviate Examiner's objections. In addition to claims 10 and 14, a thorough review of claims 8, and 11-12, and 15-16 revealed additional informalities. Thus, claims 8-10, 11-12, and 14-16 were amended to correct minor informalities present in each claims.

With regard to claim 8, claim 8 was amended to correct the following informalities : the term source region and first transistor was amended to a "drain" region (326) of the "first" transistor (360) having the second conductivity.

With regard to claim 10, claim 10 was amended to correct the following informalities: a "source" region (406) and a "drain" region (404) of the third N-type transistor. Also, the term source region was amended to define a "drain" region (364) of the "first" N-type transistor.

With regard to claim 11, claim 11 was amended to correct informalities relating to the source and drain regions of a fourth N-type transistor, in addition to changing reference from a first inverter to a "second inverter" connected to a fourth type N-type transistor.

With regard to claim 12, claim 12 was amended to correct informalities relating to the "source" of the fourth N-type transistor, as well as relating to the "input" terminal of the second inverter.

With regard to Claim 14, claim 14 was amended to clarify the source region (386) of the second N-type transistor; the source (406) and drain (404) regions of the third N-type transistor; and the first voltage input terminal (118).

With regard to Claim 15, claim 15 was amended to clarify the source and drain regions of the fourth N-type transistor and of the input and output terminals of the second inverter.

With regard to Claim 16, claim 16 was amended to clarify the source and drain regions of the fourth N-type transistor.

IV. Claim Rejections of 35 U.S.C. §102

The Examiner quoted the following section of 35 U.S.C. 102 § (b) which forms the basis for all anticipation rejections set forth in this Office action:

A person shall be entitled to a patent unless

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The Examiner rejected claims 1-2 under 35 U.S.C. 102 § (b) as being anticipated by Hong, U.S. Patent No. 5,869,987 (hereinafter "HONG").

Applicant respectfully traverses Examiner's rejections of Claims 1-2.

With regard to Claim 1, Claim 1 of the present invention has been amended to define a power-on bias circuit comprising:

a first inverter having an input terminal and an output terminal, said input terminal functions as an input terminal of said power-up bias circuit**, wherein said input terminal of said power-on bias circuit is further in electrical communication with a core voltage input terminal;**

a second inverter having an input terminal and an output terminal, said output terminal of said second inverter functions as the output terminal for said power-up bias circuit; and

a Schmitt Trigger circuit having an input terminal and an output terminal, wherein said input terminal of the Schmitt Trigger circuit is connected to said output terminal of said first inverter, said output terminal of said Schmitt Trigger circuit is connected to said input terminal of said second inverter, said first inverter, said second inverter and said Schmitt Trigger circuit are each in electrical communication with a voltage input terminal and ground**, wherein said voltage input terminal is an input/output voltage input terminal**.

Examiner allowed claims 3-9 providing that claims 3-9 be written in independent format including the limitations of any intervening claims. Accordingly, the substance of claims 2-3 have been incorporated into claim 1. Also, Claims 2-3 have been canceled. Thus, it is believed that claim 1 patentably defines over the HONG reference.

With respect to claims 4, 6, and 8, the dependency of claims 4, 6, and 8 have changed from now canceled claim 3 to claim 1 in accordance with the amendment to claim 1 and cancellation of claim 3.

Additionally, claims 10 and 14 were amended to correct minor informalities, thereby overcoming Examiner's objections to those claims. Examiner stated that "Claims 10-17 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the Schmitt Trigger circuit comprises a first (300), second (320), a third (320) P-type transistor, a first (360), second (380), and a third (400) N-type transistor having the desired connections as called for in the claims in combination with the rest of the limitations of the base claims and any intervening claims.

Claim 18 has been added to define a power-on bias circuit comprising:

a first inverter having an input terminal and an output terminal, said input terminal functions as an input terminal of said power-up bias circuit, **wherein said input terminal of said power-on bias circuit is further in electrical communication with a core voltage input terminal**;

a second inverter having an input terminal and an output terminal, said output terminal of said second inverter functions as the output terminal for said power-up bias circuit; and

a Schmitt Trigger circuit having an input terminal and an output terminal, wherein said input terminal of the Schmitt Trigger circuit is connected to said output terminal of said first inverter, said output terminal of said Schmitt Trigger circuit is connected to said input terminal of said second inverter, said first inverter, said second inverter and said Schmitt Trigger circuit are each in electrical communication with a voltage input terminal and ground.

Specifically, as Examiner admitted on OA, page 4, clause 9: the prior art of record fails to disclose a circuit as shown in FIG. 4 having an input terminal (128) of the power-on bias circuit in electrical communication with a core voltage input terminal (118).

It is believed that all pending claims, i.e., 1, and 4-18 are now in condition for allowance.

V. Conclusion

In view of the foregoing discussion, the Applicant has responded to each and every rejection of the Official Action. The Applicant has clarified the structural distinctions of the present invention by amendments herein. The foregoing discussion and amendments do not present new issues for consideration and that no new search is necessitated. Such amendments are supported by the specification and do not constitute new matter. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejections under 35 U.S.C. §102, and further examination of the present application. Should any fee be due as a result of this response, the Commissioner is hereby authorized to charge Deposit Account No. 50-0484 any such fee.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned representative to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,

Randy Tung (31,311)

MARK-UP SHEET

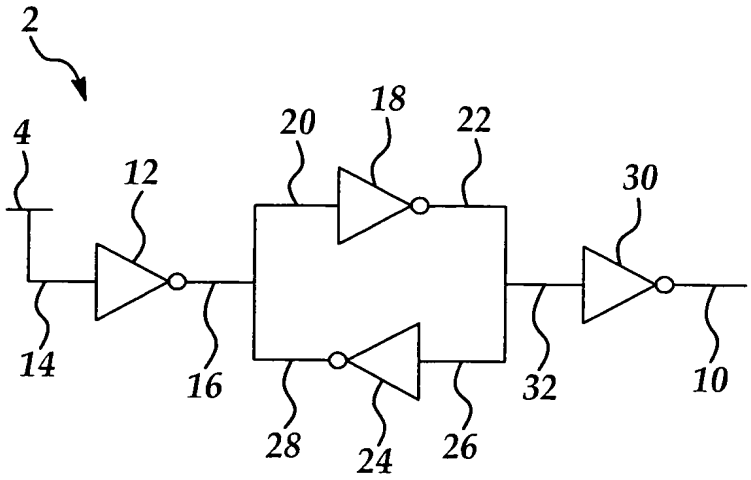

Figure 1
Prior Art

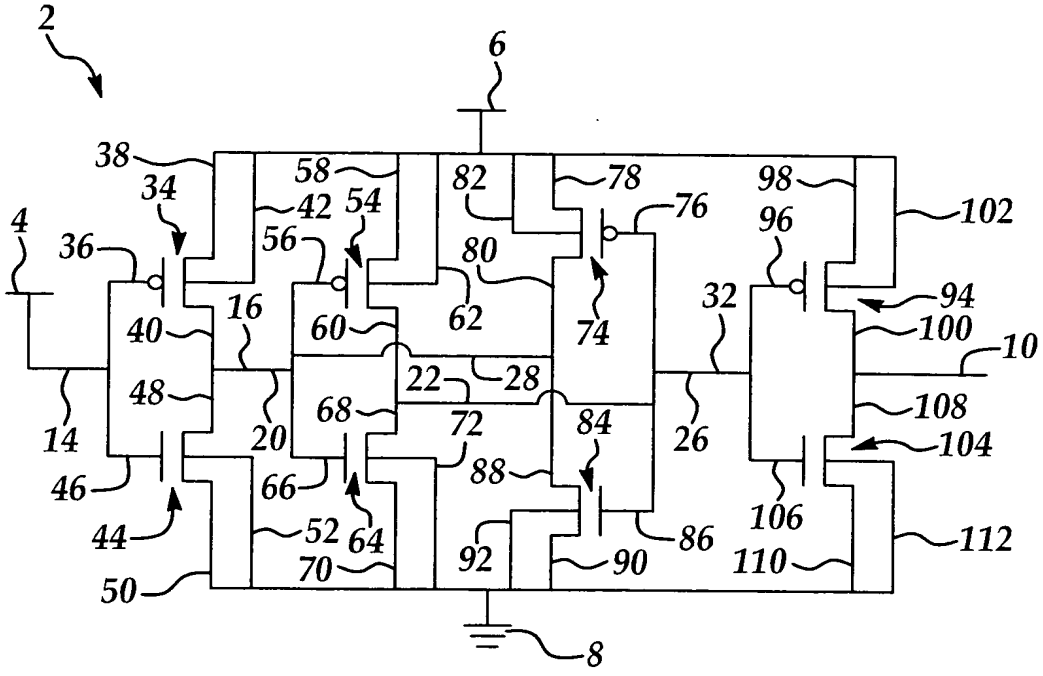

Figure 2
Prior Art